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In re Patent Application of: Alan R. Reinberg
Title: METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT
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PATENT APPLICATION TRANSMITTAL

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METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT

FIELD OF THE INVENTION

The present invention relates to fabricating electrically programmable and electrically erasable memory cells and particularly, fabricating the cells to substantially eliminate hot-electron degradation effects.

BACKGROUND

Memory circuit arrays positioned on semiconductor chips have become an important component common to VLSI circuits. Memory circuits rely upon storage of data in a memory array within a section of a chip designated for memory. The memory array is comprised of memory cells.

Memory circuits are of two basic types--volatile memory circuits and nonvolatile memory circuits. A nonvolatile memory circuit does not lose stored "bits" or information when the circuit loses power. For a volatile memory circuit, information is lost when the circuit loses power.

ROM or read-only memory is a basic type of nonvolatile memory. Data stored in ROM is a permanent part of the circuit. The ROM circuit provides precoded information to a user. One variation of ROM is an erasable programmable ROM, commonly referred to as EPROM. To create the erasable feature, a transistor, such as a memory MOS transistor, is selectively charged to impart data to the memory field. The memory field is programmed by a procedure of hot electron injection. The memory field may be re-programmed by draining off the charge, removing the chip from the circuit and imparting a new memory with an exterior source.

An improvement to EPROM is a memory circuit that can be reprogrammed while the chip is in a socket of a machine. This memory circuit, an EEPROM circuit, is prepared for reprogramming by draining charge and by charging the

memory circuit in place. The EEPROM memory circuit is programmed and reprogrammed by hot electron injection.

Both EPROM and EEPROM comprise a large number of memory cells having electrically isolated gates, referred to as floating gates. Data is stored in the memory cells in the form of charge on the floating gates. Charge is transported to or removed from the floating gates by program and erase operations, respectively.

One other type of memory circuit, a FLASH circuit, is a form of EEPROM, which is a form of electronically erasable, programmable, read only memory. FLASH memory is based upon a one-transistor cell design but has a capacity for in-socket programming and erasure. FLASH memory is a type of nonvolatile memory. FLASH memory differs from EPROM and EEPROM in that erase programs are done in blocks.

One prior art memory circuit, illustrated in FIGS. 1(a) and 1(b), comprises a memory 184 with a memory array 198, control logic 194 and address logic 196, illustrated in prior art FIG. 1(b). The address logic 196 receives an address from an external system, such as a microprocessor. The control logic 194 receives external commands to store or to retrieve data to or from the memory array 198 at cell location(s) provided to the address logic 196 by the external system. Subsequently, the data associated with cell location(s) is respectively transmitted to or received from the external system.

The memory 184 may be FLASH memory. The memory array 198 includes a plurality of FLASH cells of each having a floating gate transistor such as storage transistor 182 of FIG. 1(a). The storage transistor 182 comprises two gates, a floating gate stack 170 and a control gate stack 172, an active source region 152a and an active drain region 152b and a channel 162 also formed in the semiconductor 168. Both the floating gate stack 170 and the control gate stack 172 are formed by conductors 122 and 124 and gate oxides 144 and 146.

Nonvolatile memory storage in a circuit requires a permanent storage of charge in the floating gate stack region of the memory circuit. Nonvolatile memory storage in a memory circuit such as an EEPROM or a FLASH memory circuit is

made possible by materials used in the gate region, including materials added by doping and by structural design of the gate region. These materials include silicon of a wafer supporting the circuit and silicon oxide formed during gate fabrication.

FLASH memory is especially sensitive to degradation effects due to a substantial number of hot electrons generated in each memory cell during flash memory cycling. Specifically, during an operation of programming a memory cell, a positive programming voltage is applied to the control gate stack 172. This positive programming voltage attracts electrons from the semiconductor 168 which is a p-type substrate and causes them to accumulate at the surface of channel region 162. A voltage on drain 152b is increased and the source 152a is connected to ground. As the drain-to-source voltage increases, electrons flow from the source 152a to drain 152b via the channel region 162. As electrons travel toward drain 152b they acquire substantially large kinetic energy and are referred to as hot electrons. The hot electrons are injected through the oxide layer 146 and are stored on floating gate stack 170.

FLASH memory cycling occurs when the FLASH memory is repeatedly programmed and erased. With FLASH memory cycling, a significant number of substrate hot electrons are trapped within an insulating gate oxide layer 146, such as is shown in the prior art FLASH circuit in FIG. 1(a), that separates a drain region 152a from the floating gate stack 170. The greater the number of cycles that a FLASH memory device is subjected to, the greater the number of carriers that become trapped in the gate oxide.

The trapping and accumulation of hot electrons starts a charging process. Gradually, as the charge on the floating gate increases, the electric field in oxide layer 144 decreases and eventually loses its capability of attracting any more of the hot electrons to the floating gate 170. At this point, the floating gate stack 170 is fully charged. The negative charge from the hot electrons collected in the floating gate stack 170 raises the cell's threshold voltage above a logic 1 voltage. If the voltage on control gate stack 172 is brought to a logic 1 during a read operation, the cell will barely turn on. Sense amplifiers are used in the memory to detect and

amplify the state of the memory cell during a read operation. Thus, data is read from a memory cell based upon its "ON" characteristics.

Hot electron degradation effects have been observed in FLASH memories in two ways. Most noticeably, the erase/programming times for a given memory array are increased far beyond their normal limits. This phenomena is frequently referred to a "erasetime/programtime push-out." This means that as the devices are repeatedly cycled, a greater amount of erase/program time must be allotted for each successive cycle in order to insure that the entire array is completely charged or discharged.

A second indication that degradation effects are manifested in a FLASH memory cell array is an excess charge loss which renders the memory devices unreliable. That is, even though the device is initially programmed to an "apparently" correct level, with time that programming level may drop below the limits of reliable operation. This "apparent" charge loss of the devices occurs after extensive program-erase cycles.

Several methods have been developed in attempts to reduce hot electron induced degradation. One method uses a lightly doped drain, LDD, positioned proximal to a highly doped region. The LDD spreads an electric field in an attempt to prevent the hot electrons from gaining sufficient energy to break the silicon-hydrogen bonds. The use of an LDD reduces but does not eliminate the effects of hot electron induced degradation. Furthermore, the use of an LDD may further degrade the transistor by creating higher resistance than desired.

Another method is described in an article by F.C. Hsu et al., "Effect of Final Annealing on Hot-Electron-Induced MOSFET Degradation," IEEE Device Letters, vol. edl-6, No. 7, July 1985. A metal oxide semiconductor field effect transistor (MOSFET) as used herein refers to a field-effect transistor containing a metal gate over thermal oxide over silicon. The method described in Hsu et al. for reducing the effects of hot electron induced degradation has included a use of a nitrogen ambient rather than a hydrogen ambient to perform a final anneal in a post-metallization procedure in order to reduce the amount of hydrogen available to bond with silicon.

Although the use of the nitrogen ambient reduced the amount of hydrogen available to bond with silicon, it was difficult to eliminate hydrogen entirely, since many of the procedures employed to fabricate a MOSFET are hydrogen-dependent. Thus, while the use of nitrogen ambient reduced the amount of hydrogen present, the use did not eliminate hydrogen nor the problems caused by hot electron induced degradation.

Electrons are removed from the floating gate to erase the memory cell. Many memories, including FLASH memories, use Fowler-Nordheim (FN) tunneling to erase a memory cell. The erase program is accomplished by electrically floating the drain, grounding the source, and applying a high negative voltage to the control gate. This creates an electric field across the gate oxide and forces electrons off the floating gate. The electrons then tunnel through the gate oxide.

One of the difficulties with FLASH memories has been with the erase operation using Fowler-Nordheim tunneling. The erase operation requires high voltages, and is relatively slow. Further, an erratic over erase can be induced as a result of the very high erase voltages used. These very high erase voltages are a fundamental problem arising from the high electron affinity of bulk silicon or large grain polysilicon particles used as the floating gate. The high erase voltages create a very high tunneling barrier. Even with high negative voltages applied to the gate, a large tunneling distance is experienced with a very low tunneling probability for electrons attempting to leave the floating gate. This results in long erase times because the net flux of electrons leaving the gate is low. Thus, the tunneling current discharging the gate is low.

Other phenomena result as a consequence of this very high negative voltage. One phenomenon is hole injection. Hole injection into the oxide is experienced which can result in erratic over erase, damage to the gate oxide itself and the introduction of trapping states.

A reference of K. Hess et al., *IEEE Transactions on Electron Devices*, vol. 45, No. 2, Feb. 1998, entitled, "Giant Isotope Effect in Hot Electron Degradation of Metal Oxide Silicon Devices," at pp. 406 to 416, describes a giant

isotope effect of hot electron degradation. The effect was observed in integrated circuits of a complementary metal oxide silicon (CMOS) type. To study this effect, the authors passivated silicon wafers with deuterium instead of hydrogen.

The authors observed that the desorption efficiency for deuterium from silicon was about a factor of fifty lower than for hydrogen for energies above about 5 eV. The authors concluded that hydrogen migration played some role in mechanisms responsible for gate oxide wear-out. In particular, the authors concluded that a large deuterium content at a silicon wafer interface could be correlated to an improvement in transistor lifetime for some types of transistors. The authors attributed the longer lifetime to minimized damage occurring during a single event of hot electron injection.

With hot electron injection, the steady state of hydrogen within a silicon dioxide film is disrupted because the energy from the injection ionizes the hydrogen to H+ ions. It is believed that electrons from the hot electron injection excite or collide with hydrogen that is bound to silicon or polysilicon at the Si/SiO_2 interface. A collection of H+ ions drift to a memory storage area of the memory circuit, such as a floating gate, and combine with stored electrons.

The stored electrons are ordered within fields so as to "hold" nonvolatile memory within the circuit. Once hydronium ions are combined with electrons, hydrogen gas is formed and data within the memory is destroyed. As a consequence, the transistor is degraded.

SUMMARY OF THE INVENTION

One embodiment of the present invention comprises a method for reducing single bit data loss in a memory circuit. The method includes providing a semiconductor layer that has a surface. The semiconductor layer is exposed, at an elevated temperature, to an atmosphere comprising a vapor comprising a hydrogen isotope such as deuterium, thereby imparting deuterium on or within the semiconductor layer. A memory circuit is fabricated on or within the semiconductor layer.

In one embodiment, the high temperature treatment in a deuterium atmosphere forms a film of a thin layer of silicon dioxide. In another embodiment, the film formed is silicon nitride. In one other embodiment, the film is silicon oxynitride. For each embodiment, the film is prepared in an atmosphere that comprises deuterium. In another embodiment, the high temperature treatment with deuterium anneals the silicon surface.

Another embodiment of the present invention comprises a memory circuit that comprises a main body comprised of silicon. A memory cell is disposed on and within the main body. A gate region is proximal to the memory cell. A film is disposed on or within the gate region or under the gate region. The film comprises deuterium. The memory circuit is resistant to random single bit data loss.

Another embodiment of the present invention comprises a method of forming a non-volatile electrically alterable semiconductor memory cell. The method includes providing a silicon substrate and fabricating a field oxide region and a channel region over and within the silicon substrate. The method also includes growing an oxide over the channel region in an atmosphere enriched in deuterium, fabricating one or more gate members proximal to the oxide and passivating the memory cell in an atmosphere that comprises deuterium.

One other embodiment of the present invention comprises a thermal oxide component or a tunneling oxide component of a non-volatile, electrically alterable semiconductor memory cell that comprises deuterium.

Another embodiment of the present invention comprises a method for passivating a non-volatile, electrically alterable semiconductor memory cell. The method comprises providing a non-volatile, electrically alterable semiconductor memory cell and exposing the memory cell to an atmosphere that comprises deuterium.

Another embodiment of the present invention comprises a method for overlaying source and drain regions of a non-volatile, electrically alterable semiconductor memory cell with a thermal oxide layer. The method comprises providing a silicon substrate and defining source and drain regions. The method

also comprises growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises deuterium.

DESCRIPTION OF THE DRAWINGS

Figure 1(a) is a cross-sectional view of one prior art embodiment of a FLASH device.

Figure 1(b) is a prior art block diagram of a memory.

Figure 2 is a cross-sectional view of one embodiment of a FLASH device of the present invention.

Figure 3 is a cross-sectional view of one other embodiment of a FLASH device of the present invention.

DETAILED DESCRIPTION

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

For purposes of this specification, the terms "chip", "wafer" and "substrate" include any structure having an exposed surface of semiconductor material with which to form integrated circuit (IC) structures. These terms are also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. The terms include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known in the art. The term "conductor" is understood to include semiconductors, and the term "insulator" is defined to include any material that is less electrically conductive than the

materials referred to as "conductors." The following detailed description is, therefore, not to be taken in a limiting sense. The term "hydrogen isotope" refers to deuterium, tritium and compounds that include deuterium and tritium.

A FLASH memory circuit according to one embodiment of the present invention, illustrated generally at 200 in FIG. 2 and a memory cell of the present invention, illustrated generally at 210 in FIG. 2 are fabricated employing metal-oxide-semiconductor, MOS, technology as well as non-metal based technology utilizing materials such as polysilicon. One embodiment of a method for fabricating the FLASH memory circuit 200 utilizes MOS fabrication techniques in conjunction with a process for fabricating a FLASH memory device, i.e. EPROM, or an array which relies on hot electron injection of carriers between a substrate and a floating gate member of the memory cell.

One embodiment of the method of the present invention, for reducing low temperature single bit data loss in memory such as FLASH memory, comprises providing a silicon wafer with a silicon surface; fabricating a gate region in the wafer; and treating a portion of the silicon surface to form a thin layer of insulator film adjacent to the gate region and under the gate region. The thin layer of insulator film is prepared using an annealing medium that comprises deuterium.

The FLASH memory circuit 200 comprises the FLASH cell 210 that comprises a floating gate 204 and a control gate 202 as well as an active region 212 and a channel 214 formed in a silicon semiconductor 216. Both the floating gate 204 and control gate 202 are formed by conductors 216 and 218 and gate oxide 220 and 222. The gate oxide 220 and 222 is comprised of silicon oxide or silicon nitride or silicon oxynitride or combinations of these oxides. A hydrogen isotope such as deuterium, designated "D" in FIG. 2, is entrapped within the film. The FLASH memory circuit of the present invention is resistant to single bit data loss within its memory at low temperature.

Repeated cycling of a FLASH memory results in charge loss from the floating gate 204 and a corresponding degradation in device performance. It is believed that this phenomena is caused in part by the introduction of hydrogen into

the active regions of the field effect device. The presence of hydrogen enhances interface state generation and causes device degradation. It is also believed, that a single bit data loss type of degradation is reduced by annealing silicon regions proximal to the memory circuit in a medium enriched in deuterium, and forming the gate oxide 220 and 222 which is enriched in deuterium. The annealing is performed, in one embodiment, as a final post-metallization anneal. The anneal is performed in an atmosphere comprising approximately four percent to one-hundred percent deuterium with the remaining gas being an inert gas or nonreactive gas such as nitrogen or a combination of the inert gas and the nonreactive gas.

Intermediate anneals performed during memory circuit fabrication may also be performed in a deuterium atmosphere or other Hydrogen isotope atmosphere. These intermediate anneals include oxidation of specific memory cell layers in an atmosphere that comprises either deuterium or a compound that includes deuterium such as D_2O, D_2, or ND_3.

One other embodiment of the memory cell device of the present invention is illustrated at 300 in FIG. 3. The FLASH memory cell 300 is also fabricated utilizing metal-oxide-semiconductor, MOS, techniques. The FLASH memory cell 300 is fabricated on a p-type silicon substrate 330. Field oxide isolation regions 350 are defined using a silicon nitride masking layer. The field oxide regions 350 are then grown, in one embodiment, to a thickness of about 7500 Angstroms.

Following formation of the field oxide regions 350, a high-grade tunneling oxide 340 is thermally grown above a channel region 420 of the substrate. After that, in one embodiment, a phosphorous-doped polycrystalline silicon, polysilicon, layer 360 is deposited and etched in a pattern which will subsequently form the floating gates for each of the memory cells. After a thermally grown dielectric layer 320 is grown over layer 360, a second layer of polysilicon 370 is deposited and etched in a pattern which runs generally perpendicular to the pattern of layer 360. The second layer 370 defines the control gate for the memory device. Layer 360 forms the floating gate of the device. Control gate member 370 stretches over the

active channel region 420 of the cell and extends beyond the tunnelling region to the next cell, thereby forming a word line in an array.

The source and drain regions for the cells are formed after the polysilicon, poly 2 layer 370 has been defined. In one embodiment, an arsenic implant is used to form a source drain region. The source drain region may receive an additional phosphorous implant, thereby forming a deeper phosphorous source junction because the phosphorous diffuses into the silicon. The phosphorous implant causes the source side to have a deeper and more gradual dopant concentration gradient than the drain side. The deeper implantation reduces substrate current during electrical erase. The source drain region may also be formed by ordinary diffusion steps. Region 310 represents a common source within the FLASH memory array.

After the source and drain regions are formed, a thermal oxide layer 230 is grown over the source/drain and polysilicon gate surfaces. A CVD dielectric film 380 is then deposited on top of the thermal oxide to planarize the device.

To open the drain contact, the device is masked and etched until an area of silicon directly over the drain region is exposed. This becomes the drain contact region 340. In one embodiment, an aluminum metalization layer 400 is deposited over the device to connect the drain regions and forms the bit lines of the memory array.

The entire device is then passivated by annealing an insulating layer 410 in an atmosphere that comprises deuterium and a nitrogen ambient so that the layer 410 is comprised of oxynitride and deuterium. The insulating layer 410 may also be comprised of silicon oxide and deuterium. It is believed that forming a passivation layer that comprises deuterium retards diffusion of hydrogen atoms under the metalization layer and migration to the channel region 420. The hydrogen atoms cannot then interact with continuous charge transfer that occurs in the gate oxide region of the memory devices.

Passivation as used herein refers to a process whereby a film is grown on a surface to either chemically protect it from the environment or to provide electronic stabilization of the surface. The method of the present invention includes

embodiments wherein intermediate passivation in an atmosphere comprising deuterium is performed on layers such as 220 and 222 in FIG. 2. The method of the present invention also includes embodiments wherein a device passivation in an atmosphere comprising deuterium or other Hydrogen isotope is performed on a layer such as 410 in FIG. 3.

One conventional silicon passivation reaction, free from deuterium is the following:

$$Si\ (solid) + H_2O\ (gas) \dashrightarrow SiO_2\ (solid) + 2H_2\ (gas).$$

With the conventional silicon passivation reaction of an intermediate layer, hydrogen remaining in the oxide proximal to a gate is believed to be in a steady state relationship with the oxide. Substituting deuterium ions or other Hydrogen isotopes for protons in the process of surface silicon oxide formation in and proximal to memory storage areas such as gate regions is believed to produce a reduction in the drift of positively charged particles. In one other passivation embodiment, passivation of a silicon/silicon dioxide interface of a wafer comprises a treatment of a dangling bond with H_2 in order to make a passivated dangling bond and hydrogen gas.

The passivation reaction using deuterium or other Hydrogen isotope in order to form silicon dioxide, is as follows:

$$Si\ (solid) + D_2O\ (gas) \dashrightarrow SiO_2\ (solid) + 2\ D_2\ (gas).$$

Passivation utilizing one embodiment of the method of the present invention is performed in a deuterium or other Hydrogen isotope atmosphere at a temperature of 400° C to 450° C for 0.5 to 2 hours. The percentage of deuterium in the passivating gas is at least about 10 percent by volume and may be about 100 percent. Other non-reactive components of the passivation gas include helium or nitrogen gas. The passivation occurs as a consequence of annealing the silicon/silicon dioxide surface of the semiconductor wafer. In addition to this thermal oxidation-based method, deuterium may be introduced into a silicon dioxide layer by pyrolytic diffusion from the gas or from a plasma or RF sputter deposition.

Hydrogen is replaced by deuterium in a silicon nitride film by exposing a silicon substrate to ammonia in an atmosphere enriched in deuterium at a temperature range of 950° C to 1200° C. In one embodiment, the ammonia is present as a component in a gaseous mixture of deuterium with 30 percent by volume ammonia.

Silicon oxynitride films, SiOxNy, are formed by nitridation of silicon oxide films. These films may be made with D_2, D_2O and ND_3 in order to replace hydrogen in the films with deuterium. This film array is made by utilizing the reactants D_2, D_2O and ND_3 in sequential reactions. The sequential reactions are for the preparation of silicon dioxide and silicon nitride layers of the film sandwich. Deuterium may also be introduced in or proximal to the gate region by targeted deuterium treatment, such as ion implantation, in a particular oxide and by annealing the entire device in a deuterium atmosphere.

It is to be appreciated that the method and memory circuit of the present invention have been described in particular detail with respect to preferred processes and structures. The present invention, however, is not intended to be limited to these preferred embodiments. One skilled in the art will readily recognize that the actual method and circuit may be adjusted to accommodate particular conditions.

What is claimed is:

1. A method for reducing random single bit data loss in a memory circuit comprising:

providing a semiconductor layer having a surface;

heating the layer in an atmosphere comprising a Hydrogen isotope; and

fabricating a memory circuit using the semiconductor layer.

2. The method of claim 1 and further comprising forming a film on the semiconductor layer that comprises the Hydrogen isotope.

3. The method of claim 1 and further comprising fabricating a FLASH memory circuit using the semiconductor layer.

4. The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that oxidizes the semiconductor layer.

5. The method of claim 1 and further comprising exposing the semiconductor layer to a temperature that anneals the semiconductor layer.

6. The method of claim 1 and further comprising exposing the semiconductor, sequentially, to atmospheres comprising Hydrogen isotope and ammonia enriched in Hydrogen isotope at an elevated temperature.

7. The method of claim 1 and further comprising fabricating a gate region within the memory circuit.

8. The method of claim 7 and further comprising forming a film comprising Hydrogen isotope adjacent to the gate region of the memory circuit.

9. The method of claim 7 and further comprising forming a film comprising Hydrogen isotope within the gate region of the memory circuit.

10. The method of claim 1 and further comprising passivating the semiconductor layer in an atmosphere comprising Hydrogen isotope.

11. The method of claim 1 and further comprising forming a field oxide in the semiconductor layer.

12. The method of claim 11 and further comprising annealing the field oxide layer in an atmosphere that comprises Hydrogen isotope or a Hydrogen isotope containing compound.

13. The method of claim 11 and further comprising annealing at a temperature that is at least about 800 degrees Centigrade.

14. The method of claim 11 and further comprising oxidizing the annealed field oxide layer in an atmosphere that comprises Hydrogen isotope.

15. An annealing atmosphere for annealing a semiconductor device with a FLASH memory comprising Hydrogen isotope and or a compound that comprises Hydrogen isotope.

17. The annealing atmosphere of claim 15 and further comprising water vapor.

18. The annealing atmosphere of claim 15 and further comprising an inert gas.

19. The annealing atmosphere of claim 15 and further comprising nitrogen or a compound comprising nitrogen.

20. A memory circuit, comprising:

a main body comprising silicon;

a memory cell disposed on and within the main body;

a gate region proximal to the memory cell disposed on and within the main body; and

a film disposed on or within the gate region, adjacent to the gate region or under the gate region, wherein the film comprises Hydrogen isotope.

21. The memory circuit of claim 20 wherein the memory cell is a FLASH memory.

22. The memory circuit of claim 20 wherein the film is a silicon dioxide film comprising Hydrogen isotope.

23. The memory circuit of claim 20 wherein the film is a silicon nitride film comprising Hydrogen isotope.

24. The memory circuit of claim 20 wherein the film comprises silicon dioxide and silicon nitride and Hydrogen isotope.

25. The memory circuit of claim 20 wherein the film comprises silicon oxynitride.

26. A method of forming a non-volatile electrically alterable semiconductor memory cell comprising:

providing a silicon substrate;

fabricating a field oxide region and a channel region over or within the silicon substrate;

growing an oxide over the channel region in an atmosphere enriched in Hydrogen isotope;

fabricating at least one gate member; and

passivating the memory cell in an atmosphere that comprises Hydrogen isotope.

27. The method of claim 26 and further including nitridizing the field oxide region by annealing in an atmosphere comprising Hydrogen isotope or a compound that comprises Hydrogen isotope.

28. The method of claim 26 and further comprising nitridizing at a temperature that is greater than or equal to about 800 degrees Centigrade.

29. The method of claim 26 and further including oxidizing the nitridized field layer in an atmosphere that comprises Hydrogen isotope.

30. The method of claim 26 and further comprising introducing the Hydrogen isotope by thermal oxidation.

31. The method of claim 26 and further comprising introducing the Hydrogen isotope by pyrolytic diffusion of Hydrogen isotope into the memory cell.

32. The method of claim 26 and further comprising introducing the Hydrogen isotope by RF sputter deposition.

33. A tunneling oxide component of a non-volatile, electrically alterable semiconductor memory cell, comprising Hydrogen isotope.

34. A thermal oxide component of a non-volatile, electrically alterable semiconductor memory cell, comprising Hydrogen isotope.

35. A method for passivating a non-volatile, electrically alterable semiconductor memory cell, comprising:

providing a non-volatile, electrically alterable semiconductor memory cell; and

exposing the memory cell to an atmosphere that comprises Hydrogen isotope.

36. The method of claim 35 and further including heating the atmosphere.

37. A method for overlaying source and drain regions of a non-volatile, electrically alterable semiconductor memory cell with a thermal oxide layer, comprising:

providing a silicon substrate;

defining source and drain regions; and

growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises Hydrogen isotope.

38. The method of claim 37 and further comprising heating the atmosphere that comprises Hydrogen isotope.

39. The method of claim 37 and further comprising defining the source and drain regions by targeted Hydrogen isotope implantation.

ABSTRACT

The present invention includes a method for reducing random bit data loss in a memory circuit. The method comprises a semiconductor layer that has a surface. The semiconductor layer is exposed at an elevated temperature to an atmosphere comprising deuterium thereby forming a film on the semiconductor layer comprising deuterium. A memory circuit is fabricated on or within the semiconductor layer.

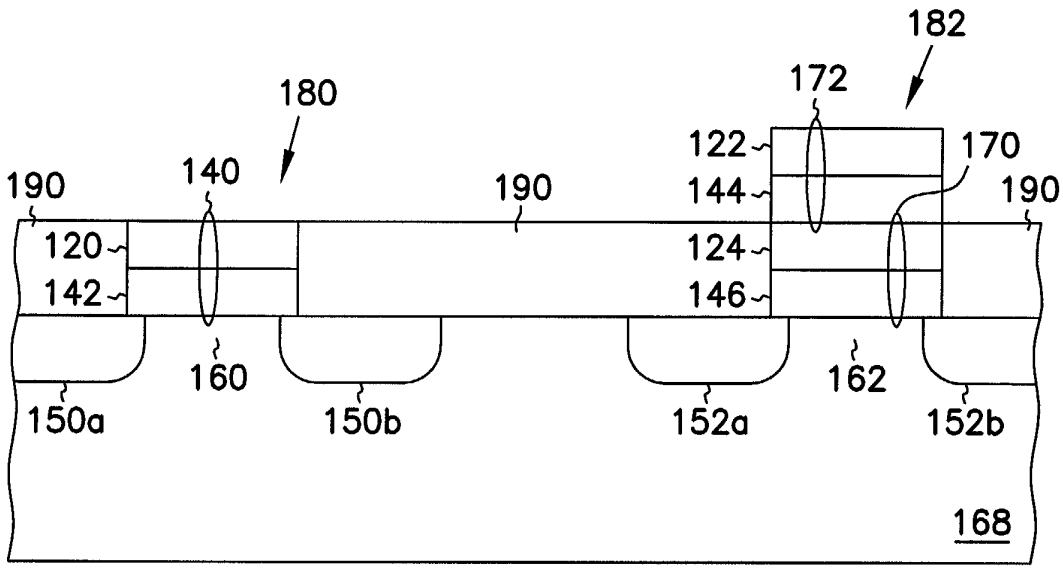

FIG. 1a
(PRIOR ART)

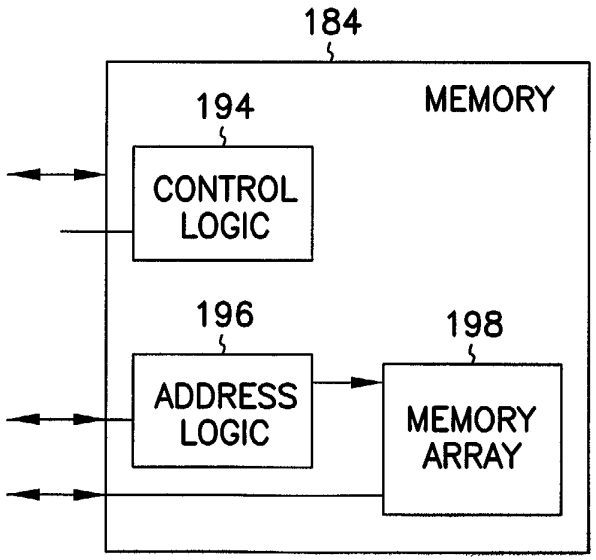

FIG. 1b
(PRIOR ART)

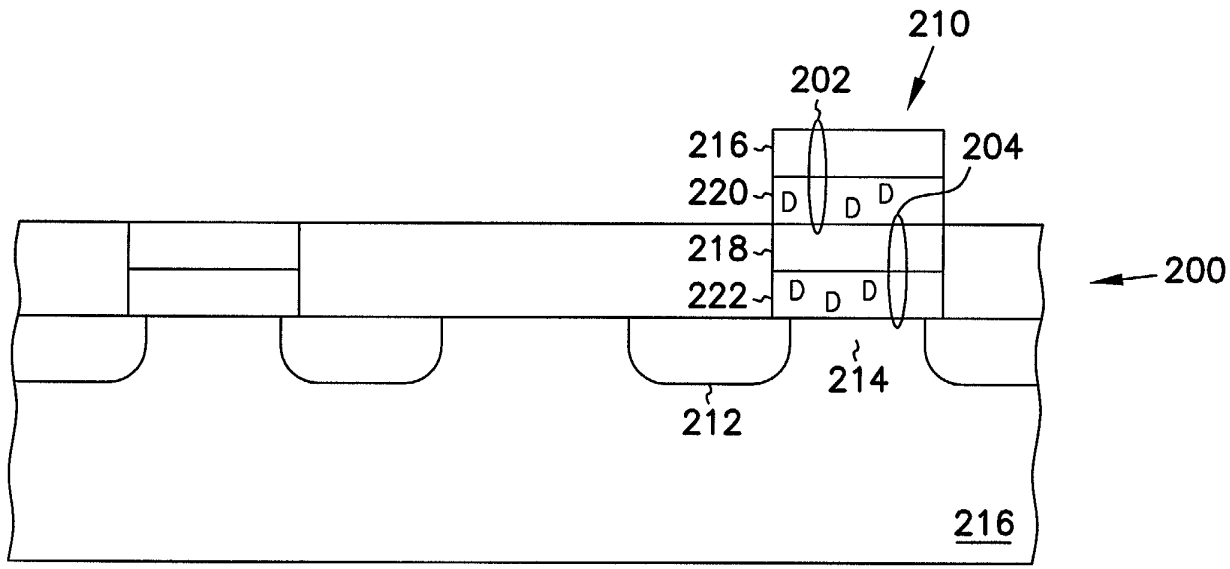

FIG. 2

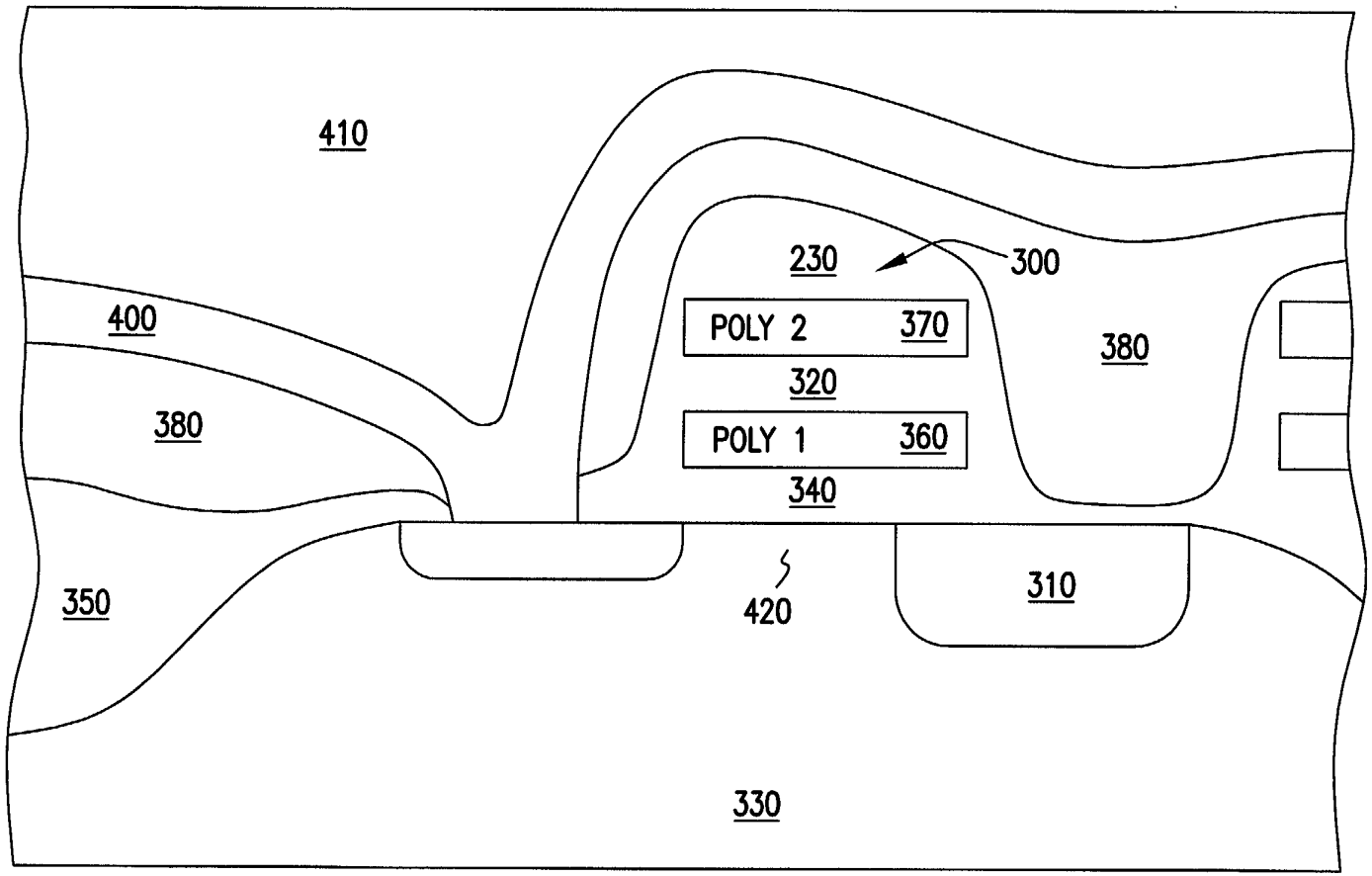
410
230
300
400
POLY 2
370
380
320
380
POLY 1
360
340
350
420
310
330

FIG. 3

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Alan R. Reinberg**
Citizenship: **United States of America** Residence: **Westport, CT**
Post Office Address: 6 Terhune Drive
Westport, CT 06880

Signature: _____ Date: August 12, 1999
Alan R. Reinberg

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

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§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Alan R. Reinberg	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 303.522US1	
Title:	METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Adams, Gregory J.	Reg. No. P-44,494	Forrest, Bradley A.	Reg. No. 30,837	McCrackin, Ann M.	Reg. No. 42,858
Adams, Matthew W.	Reg. No. 43,459	Harris, Robert J.	Reg. No. 37,346	Nama, Kash	Reg. No. 44,255
Anglin, J. Michael	Reg. No. 24,916	Huebsch, Joseph C.	Reg. No. 42,673	Nelson, Albin J.	Reg. No. 28,650
Arora, Suneel	Reg. No. 42,267	Jurkovich, Patti J.	Reg. No. P-44,813	Nielsen, Walter W.	Reg. No. 25,539
Bianchi, Timothy E.	Reg. No. 39,610	Kalis, Janal M.	Reg. No. 37,650	Oh, Allen J.	Reg. No. 42,047
Billion, Richard E.	Reg. No. 32,836	Kaufmann, John D.	Reg. No. 24,017	Padys, Danny J.	Reg. No. 35,635
Black, David W.	Reg. No. 42,331	Klima-Silberg, Catherine I.	Reg. No. 40,052	Parker, J. Kevin	Reg. No. 33,024
Brennan, Thomas F.	Reg. No. 35,075	Kluth, Daniel J.	Reg. No. 32,146	Peacock, Gregg A.	Reg. No. P-45,001
Brooks, Edward J., III	Reg. No. 40,925	Lacy, Rodney L.	Reg. No. 41,136	Polglaze, Daniel J.	Reg. No. 39,801
Chu, Dinh C.P.	Reg. No. 41,676	Leffert, Thomas W.	Reg. No. 40,697	Prout, William F.	Reg. No. 33,995
Clark, Barbara J.	Reg. No. 38,107	Lemaire, Charles A.	Reg. No. 36,198	Schwegman, Micheal L.	Reg. No. 25,816
Dahl, John M.	Reg. No. P-44,639	Litman, Mark A.	Reg. No. 26,390	Sieffert, Kent J.	Reg. No. 41,312
Drake, Eduardo E.	Reg. No. 40,594	Lundberg, Steven W.	Reg. No. 30,568	Slifer, Russell D.	Reg. No. 39,838
Eliseeva, Maria M.	Reg. No. 43,328	Mack, Lisa K.	Reg. No. 42,825	Steffey, Charles E.	Reg. No. 25,179
Embretson, Janet E.	Reg. No. 39,665	Maki, Peter C.	Reg. No. 42,832	Terry, Kathleen R.	Reg. No. 31,884
Fogg, David N.	Reg. No. 35,138	Malen, Peter L.	Reg. No. P-44,894	Viksnins, Ann S.	Reg. No. 37,748
Forstenbacher, Paul J.	Reg. No. 42,546	Mates, Robert E.	Reg. No. 35,271	Woessner, Warren D.	Reg. No. 30,440

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Schwegman, Lundberg, Woessner & Kluth, P.A.
Attn: Janal M. Kalis
P.O. Box 2938
Minneapolis, MN 55402

Telephone: (612) 373-6976
Facsimile: (612) 339-3061

Dated: 8-24-1999

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel